CLAIMS

What is claimed is:

1. A method of checking digital information for a transmission error, comprising the steps of:
   a) receiving said digital information comprising data and at least one non-data portion, said data comprising a plurality of data portions, each having a fixed first length;
   b) removing said at least one non-data portion; and
   c) if said data does not include a remainder having a second length less than said first length, then checking said plurality of data portions for a transmission error; but if said data includes said remainder, then adding a zero-pad vector to said remainder to generate a zero-padded data portion having said first length, and checking said plurality of data portions and said zero-padded data portion for a transmission error.

2. The method of Claim 1, wherein said first fixed length comprises 2^n bits, where n is an integer of from 3 to 10.

3. The method of Claim 1, wherein said digital information comprises a packet or frame.

4. The method of Claim 3, wherein said packet or frame comprises $(2^x \cdot y) + z$ words, wherein 2^x is the number of words in a line of information in said packet or frame, x is an integer of from 0 to 4, y the number of lines of information in said packet or frame, and z is an integer of less than 2^x.

5. The method of Claim 3, wherein said at least one non-data portion comprises a header having a variable or fixed third length, said third length being less than or equal to said first length.

6. The method of Claim 5, wherein said removing step comprises removing at least a portion of said header and inserting said zero-pad vector therefor, such that said zero-pad vector has a length equal to that of said removed header portion.

7. The method of Claim 6, wherein said header portion has a fixed second length, and said second length is less than said first length.

8. The method of Claim 7, wherein said second length consists of 2^m bits, where m is an integer of from 3 to 8.

9. The method of Claim 7, wherein remainder has a length consisting of a difference between said first length and said second length.

10. The method of Claim 9, wherein said checking step comprises checking each of said data portions and said zero-padded data portion with common circuitry.

11. The method of Claim 1, wherein said digital information comprises serial digital information.

12. The method of Claim 1, wherein said checking step comprises calculating cyclic redundancy code (CRC) on all of said data portions and said zero-padded data portion.

13. A circuit for determining an information transmission error, comprising:

a) a first logic circuit configured to detect non-data information;

b) a zero-fill circuit configured to replace at least a portion of said non-data information with a zero-pad vector; and

c) an error detection circuit configured to (i) detect a transmission error in data portions of said information and a zero-padded data portion of said information, said data portions and said zero-padded data portion having a first fixed bit length, and (ii) combine said zero-pad vector with a remaining data portion of said information to form said zero-padded data portion.

14. The circuit of Claim 13, wherein said first fixed bit length is 2^n bits, where n is an integer of from 3 to 10.

15. The circuit of Claim 13, wherein said information comprises a packet or frame.

16. The circuit of Claim 15, wherein said non-data information comprises a header portion having a variable length or a second fixed length, said variable length and said second fixed length each being less than or equal to said first fixed length.

17. The circuit of Claim 16, wherein said header portion has said second fixed length, and said second fixed length is less than said first fixed length.

18. The circuit of Claim 17, wherein said second fixed length consists of 2^m bits, where m is an integer of from 3 to 8.

19. The circuit of Claim 13, further comprising a second logic circuit configured to remove said portion of said non-data information and insert said zero-pad vector for at least part of said portion of said non-data information.

20. The circuit of Claim 13, wherein said error detection circuit comprises a cyclic redundancy checking (CRC) circuit.

21. The circuit of Claim 13, further comprising a control circuit configured to transmit a control signal in response to said error detection circuit detecting (i) an error in said data portions and said zero-padded data portion of said information, or (ii) no error in said data portions and said zero-padded data portion of said information.

22. The circuit of Claim 13, further comprising a processor configured to process said data portions of said information received from said error detection circuit.

23. The circuit of Claim 22, wherein said processor is further configured to reassemble said non-data portion and said data portions of said information.

24. The circuit of Claim 13, further comprising a deserializer configured to convert serial information into parallel information for processing by said first circuit and said error detection circuit.

25. The circuit of Claim 13, further comprising a decoder configured to decode at least part of said non-data information.

26. The circuit of Claim 25, wherein said information comprises serial information, and said decoder is further configured to receive said serial information.

27. A receiver, comprising:
    a) the circuit of Claim 13;
    b) a processor in communication with said circuit, configured to process said data portions; and

c) a clock recovery circuit configured to recover a clock signal from serial information received by said receiver.

28. The receiver of Claim 27, embodied on a single integrated circuit.

29. The receiver of Claim 27, further comprising a divider configured to divide said recovered clock.

30. A system for transferring data on or across a network, comprising:

a) the receiver of Claim 27;

b) at least one transmitter in communication with said receiver, said transmitter being configured to transmit said serial information to said receiver; and

c) at least one receiver port in communication with said receiver for receiving said serial information.

31. The system of Claim 30, wherein said transmitter further comprises (i) a CRC calculator configured to calculate CRC information and (ii) a transmitter processor configured to add said CRC information to or insert said CRC information in said non-data information.

32. The system of Claim 30, wherein said receiver further comprises a control circuit configured to generate a control signal in response to said error detection circuit detecting (i) an error in said data portions and said zero-padded data portion of said information, or (ii) no error in said data portions and said zero-padded data portion of said information.

33. The system of Claim 32, further comprising a control bus configured to transmit said control signal from said receiver to said transmitter.

34. A fabric adapter or fabric processor comprising the system of Claim 30.

35. A network, comprising:

a) a plurality of the systems of Claim 30, in communication with each other; and

b) a plurality of storage or communications devices, each of said storage or communications devices being in communication with one of said systems.

36. The network of Claim 35, wherein said plurality of storage or communications devices comprises a plurality of storage devices.

37. A circuit for determining an information transmission error, comprising:

a) means for detecting non-data information;

b) means for removing at least a portion of said non-data information;

c) means for combining a zero-pad vector with a remaining data portion of said information to form a zero-padded data portion; and

d) means for detecting a transmission error in both (i) data portions of said information and (ii) said zero-padded data portion of said information, said data portions and said zero-padded data portion having a first fixed bit length.

38. The circuit of Claim 37, wherein said first fixed bit length is 2^n bits, where n is an integer of from 3 to 10.

39. The circuit of Claim 37, wherein said information comprises a packet or a frame.

40. The circuit of Claim 39, wherein said information comprises said packet, and said non-data portion comprises a packet header.

41. The circuit of Claim 40, wherein said removed portion of said packet header has said second fixed length, and said second fixed length is less than said first fixed length.

42. The circuit of Claim 41, wherein said second fixed length consists of 2^m bits, where m is an integer of from 3 to 8.

43. The circuit of Claim 37, wherein said means for detecting said transmission error comprises a means for calculating cyclic redundancy code (CRC) on said data portions and said zero-padded data portion of said information.

44. The circuit of Claim 37, further comprising a means for transmitting a control signal in response to an error detected in said data portions and said zero-padded data portion of said information.

45. The circuit of Claim 37, further comprising a means for processing said data portions of said information received from said error detection circuit.

46. The circuit of Claim 45, wherein said means for processing comprises a means for reassembling replaced non-data portion(s) and said data portions of said information.

47. The circuit of Claim 37, further comprising a means for converting serial information into parallel information for processing by said means for detecting non-data information and said error detection circuit.

48. The circuit of Claim 37, further comprising a means for decoding at least part of said non-data information.

49. A receiver, comprising:

a) the circuit of Claim 37;

b) a means for processing at least said data portions of said information, in communication with said circuit; and

c) a means for recovering a clock signal from serial information received by said receiver.

50. The receiver of Claim 49, embodied on a single integrated circuit.

51. The receiver of Claim 49, further comprising a means for dividing said recovered clock.

52. A system for transferring data on or across a network, comprising:

a) the receiver of Claim 49;

b) at least one means for transmitting serial information to said receiver; and

c) at least one means for receiving said serial information, said means for receiving being communicatively coupled to said receiver.

53. The system of Claim 52, wherein said means for transmitting further comprises (1) a means for calculating CRC information and (ii) a means for adding said CRC information to or inserting said CRC information in said non-data information.

54. The system of Claim 52, wherein said receiver further comprises a means for generating a control signal in response to said means for detecting said transmission error detecting (i) an error in said data portions and said zero-padded data portion of said information, or (ii) no error in said data portions and said zero-padded data portion of said information.

55. A fabric adapter or fabric processor comprising the system of Claim 52.

56. A network, comprising:

a) a plurality of the systems of Claim 52, in communication with each other; and

b) a plurality of discrete means for storing or communicating data, each of said discrete means for storing or communicating data being in communication with at least one of said systems.

57. The network of Claim 56, wherein said plurality of discrete means for storing or communicating data comprises a plurality of discrete means for storing data.

58. A computer-readable medium or waveform containing a set of instructions which, when executed by a signal processing device configured to execute computer-readable instructions, is configured to perform the method of claim 1.

59. The computer-readable medium or waveform of Claim 58, wherein said digital information comprises a packet or frame.

60. The computer-readable medium or waveform of Claim 59, wherein said packet or frame comprises $(2^x \cdot y) + z$ words, wherein 2^x is the number of words in a line of information in said packet or frame, x is an integer of from 0 to 4, y the number of lines of information in said packet or frame, and z is an integer of less than 2^x.

61. The computer-readable medium or waveform of Claim 58, wherein removing step comprises removing at least part of said non-data portion and inserting said zero-pad vector therefor, such that said zero-pad vector has a length equal to that of said removed part of said non-data portion.

62. The computer-readable medium or waveform of Claim 58, wherein remainder has a length consisting of a difference between said first length and said second length.

63. The computer-readable medium or waveform of Claim 58, wherein said checking step comprises calculating cyclic redundancy code (CRC) on all of said data portions and said zero-padded data portion.